selected only one sector of the flash memory 12B is erased. The other mode is a block unit erasing mode that the selected single block or plural block corresponding to the selected range of the flash memory 12B is erased.

The block unit 40 is total 8K byte comprised of 64 sectors as shown from 42-1 to 42-64. Each sector from 42-1 to 42-64 is connected to a MOS transistor in order to apply erasing voltage Verase to the memory device of the each sector. Gate electrode of the each MOS transistor from 44-1 to 44-64 is connected to NOR circuit and OR circuit from 46-1 to 46-64. Sector select signal and block select signal are applied to the gate electrode of the each MOS transistor from 44-1 to 44-64 via the NOR circuit and OR circuit from 46-1 to 46-64.

When the block unit-erasing mode is selected, the corresponding command is applied to a state machine 52 by way of a command register 50. Sequentially, the command is applied to the registers 54 corresponding to single or plural block of the selected range from first block to end lock and is stored in registers 54 of each block. When the command is applied to the registers 54 corresponding to the selected range, a counter 56 sequentially designates the blocks. The block select signal is applied to the each block via the NOR circuit and OR circuit from 46-1 to 46-64. Finally, when the certain selected blocks receive the block select signal, block unit with the turn that received the signal carries out the erasing operation. If the single block is selected, the erasing operation of a single block unit is also possible.

When the sector unit-erasing mode is selected, the corresponding command is applied to the state machine 52 by way of the command register 50. Sequentially, the command is applied to the registers 54 of the selected block and is stored in registers 54. When the command is applied to the registers 54, the counter 56 designates the block. The sector unit signal is applied to the block via the NOR circuit and the OR circuit from 46-1 to 46-64. Finally, when the selected block receive the sector unit signal, the erasing operation is carried out. If the plural sector in the above block is selected, the erasing operation of plural sector is also possible.

Now referring to FIG. 5, as for the capacity between the flash memory 12A and the flash memory 12B, various combinations are conceivable by the usage of the user. The present invention is capable of employing various combination of the capacity between the above flash memories.

Referring to FIG. 5(A), the flash memory 12A which is divided into 5 sectors is 2.5 M bytes and the flash memory 12B is divided into 3 sectors is 1.5 M bytes. The total capacity of the memory is 4-M bytes. The flash memory 12A employs a range of address from 00 to 4FFFF of the address space for storing programming software. On the other hand, the flash memory 12B employs a range of address from 00 to 2FFFF for storing data.

Referring to FIG. 5(B), the flash memory 12A which is divided into 8 sectors is 4 M bytes and the flash memory 12B is divided into 5 sectors is 2.5 M bytes. The total capacity of the memory is 6.5-M bytes. The flash memory 12A employs a range of address from 00 to 7FFFF of the address space for storing programming software. On the other hand, the flash memory 12B employs a range of address from 00 to 4FFFF for storing data.

Referring to FIG. 5(C), the flash memory 12A which is divided into 14 sectors is 7 M bytes and the flash memory 12B is divided into 6 sectors is 3 M bytes. The total capacity of the memory is 10-M bytes. The flash memory 12A employs a range of address from 00 to DFFFF of the address space for storing programming software. On the other hand, the flash memory 12B employs a range of address from 00 to 5FFFF for storing data.

The present invention is capable of employing various combination of the capacity of the flash memories 12A and 12B.

Referring to FIG. 6, the present invention is capable of employing divided capacity areas of a flash memory as alternation of the flash memories 12A and 12B.

The single flash memory is divided into a program store area and a data store area. The program store area and the data store area are allocated to deferent range of the address in the single flash memory.

The exchange of between the program store area and the data store area is carried out by the /PFE signal and /DFE signal as same as the above embodiment.

It is to be understood, however, that even though numerous characteristics and advantages of the present invention have been set forth in the foregoing description, together with details of the structure and function of the invention, the disclosure is illustrative only, and changes may be made in detail, especially in matters of shape, size and arrangement of parts, as well as implementation in software, hardware, or a combination of both within the principles of the invention to the full extent indicated by 10 the broad general meaning of the terms in which the appended claims are expressed.

The present document incorporates by reference the entire contents of Japanese priority document, 09-149975 filed in Japan on May 23, 1997.

What is claimed is:

1. A flash memory device comprising:

a first flash memory array having a first predetermined number of blocks; and

a second flash memory array having a second predetermined number of blocks and sharing input/output lines with the first flash memory array, wherein the first predetermined number of blocks is different than the second predetermined number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein a read operation is enabled in the first flash memory array when the second flash memory array is written or erased.

2. The flash memory device as recited in claim 1, wherein the first flash memory array stores data and the second flash memory array stores program.

3. The flash memory device as recited in claim 1, further comprising internal program/erase control circuitry for inputting to and erasing from the first and second flash memory arrays.

4. The flash memory device as recited in claim 1, wherein the first flash memory array and the second flash memory array may be erased electrically at block level.

5. A flash memory device comprising:

a first flash memory array having a first number of blocks of storage capacity; and

a second flash memory array having a second number of blocks of storage capacity and sharing input/output lines with the first flash memory array, wherein the first number of blocks is different than the second number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein the first flash memory array is capable of being read when the second flash memory array is written or erased.

6. The flash memory device as recited in claim 5, further comprising internal program/erase control circuitry for inputting to and erasing from the first and second flash memory arrays.

7. The flash memory device as recited in claim 5, wherein the first flash memory array and the second flash memory array may be erased electrically at block level.

8. A flash memory including an array of blocks divided into multiple areas, said flash memory comprising:

a first flash memory area having a first number of blocks; and

a second flash memory area having a second number of blocks and sharing input/output lines with the first flash memory area, wherein the first number of blocks is different than the second number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein while programming or erasing in the second flash memory area, read operations are possible in the first flash memory area.

9. The flash memory as recited in claim 8, further comprising internal program/erase control circuitry for inputting to and erasing from the first and second flash memory areas.

10. The flash memory as recited in claim 8, wherein the first flash memory area and the second flash memory area may be erased electrically at block level.

11. A flash memory device comprising:

a first flash memory area;

a first X decoder and a first Y decoder for selecting a word line and a data line based on an input address, for controlling access to and from the first flash memory area;

a first latch for latching data being input to or output from the first flash memory area

a second flash memory area;

a second X decoder and a second Y decoder for selecting a word line and a data line based on the input address, for controlling access to and from the first flash memory area;

a second latch for latching data being input to or output from the second flash memory area, the first and second latches controlling a flow of data to and from input/output lines; and

a common address latch for latching address data to the first X decoder and the first Y decoder and to the second X decoder and the second Y decoder.

12. The flash memory device as recited in claim 11, wherein while programming or erasing in the second flash memory area, read operations are possible in the first flash memory area.

13. A flash memory device comprising:

a first flash memory array having a first predetermined number of sectors; and

a second flash memory array having a second predetermined number of sectors and sharing input/output lines with the first flash memory array, wherein the first predetermined number of sectors is different than the second predetermined number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein a read operation is enabled in the first flash memory array when the second flash memory array is written or erased.

14. The flash memory device as recited in claim 13, wherein the first flash memory array stores data and the second flash memory array stores program.

15. The flash memory device as recited in claim 13, further comprising internal program/erase control circuitry for inputting to and erasing from the first and second flash memory arrays.

16. The flash memory device as recited in claim 1, wherein the first flash memory array and the second flash memory array may be erased electrically at sector level.

17. A flash memory device comprising:

a first flash memory array having a first number of sectors of storage capacity; and

a second flash memory array having a second number of sectors of storage capacity and sharing input/output lines with the first flash memory array, wherein the first number of sectors is different than the second number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein the first flash memory array is capable of being read when the second flash memory array is written or erased.

18. The flash memory device as recited in claim 17, further comprising internal program/erase control circuitry for inputting to an erasing from the first and second flash memory arrays.

19. The flash memory device as recited in claim 17, wherein the first flash memory array and the second flash memory array may be erased electrically at sector level.

20. A flash memory including an array of storage divided into multiple areas, said flash memory comprising:

a first flash memory area having a first number of sectors; and

a second flash memory area having a second number of sectors and sharing input/output lines with the first flash memory area, wherein the first number of sectors is different than the second number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein while programming or erasing in the second flash memory area, read operations are possible in the first flash memory area.

21. The flash memory as recited in claim 20, further comprising internal program/erase control circuitry for inputting to and erasing from the first and second flash memory areas.

22. The flash memory as recited in claim 20, wherein the first flash memory area and the second flash memory area may be erased electrically at sector level.

23. A flash memory device comprising:

a first flash memory array having a first predetermined number of blocks; and

a second flash memory array having a second predetermined number of blocks and sharing input/output lines with the first flash memory array, wherein the first predetermined number of blocks is different than the second predetermined number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

24. A flash memory device comprising:

a first flash memory array having a first number of blocks of storage capacity; and

a second flash memory array having a second number of blocks of storage capacity and sharing input/output lines with the first flash memory array, wherein the first number of blocks is different than the second number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

25. A flash memory including an array of blocks divided into multiple areas, said flash memory comprising:

a first flash memory area having a first number of blocks; and

a second flash memory area having a second number of blocks and sharing input/output lines with the first flash

memory area, wherein the first number of blocks is different than the second number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

26. A flash memory device comprising:

a first flash memory array having a first predetermined number of sectors; and

a second flash memory array having a second predetermined number of sectors and sharing input/output lines with the first flash memory array, wherein the first predetermined number of sectors is different than the second predetermined number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein ;an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

27. A flash memory device comprising:

a first flash memory array having a first number of sectors of storage capacity; and

a second flash memory array having a second number of sectors of storage capacity and sharing input/output lines with the first flash memory array, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

28. A flash memory including an array of storage divided into multiple areas, said flash memory comprising:

a first flash memory area having a first number of sectors; and

a second flash memory area having a second number of sectors and sharing input/output lines with the first flash memory area, wherein the first number of sectors is different than the second number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

29. A flash memory device comprising:

a first flash memory array having a first predetermined number of blocks; and

a second flash memory array having a second predetermined number of blocks sharing input/output lines with the first flash memory array, wherein the first predetermined number of blocks is different than the second predetermined number of blocks, wherein each block is a minimum erasing unit of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

30. A flash memory device comprising:

a first flash memory array having a first number of blocks of storage capacity; and

a second flash memory array having a second number of blocks of storage capacity and sharing input/output lines with the first flash memory array, wherein the first number of blocks is different than the second number of blocks, wherein each block is a minimum erasing unit of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

31. A flash memory including an array of blocks divided into multiple areas, said flash memory comprising:

a first flash memory area having a first number of blocks; and

a second flash memory area having a second number of blocks and sharing input/output lines with the first flash memory area, wherein the first number of blocks is different than the second number of blocks, wherein each block is a minimum erasing unit of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

32. A flash memory device comprising:

a first flash memory array having a first predetermined number of sectors; and

a second flash memory array having a second predetermined number of sectors and sharing input/output lines with the first flash memory array, wherein the first predetermined number of sectors is different than the second predetermined number of sectors, wherein each sector is a minimum erasing unit of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

33. A flash memory device comprising:

a first flash memory array having a first number of sectors of storage capacity; and

a second flash memory array having a second number of sectors of storage capacity and sharing input/output lines with the first flash memory array, wherein the first number of sectors is different than the second number of sectors, wherein each sector is a minimum erasing unit of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

34. A flash memory including an array of storage divided into multiple areas, said flash memory comprising:

first flash memory area having a first number of sectors; and

a second flash memory area having a second number of sectors and sharing input/output lines with the first flash memory area, wherein the first number of sectors is different than the second number of sectors, wherein each sector is a minimum erasing unit of the flash memory device, and wherein an operation for reading from the second flash memory array is enabled by its respective enable line when the first flash memory array is accessed.

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